

SECOND SUPPLEMENTAL FORM PTO-1449	SERIAL NO. 10/518,291	CASE NO. 10808/195 (In1242WOUS)
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	FILING DATE December 16, 2004	GROUP ART UNIT 2825
APPLICANTS: KOEDER et al.		

EXAMINER INITIAL	OTHER ART – NON PATENT LITERATURE DOCUMENTS (Include name of author, title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date page(s), volume-issue number(s), publisher, city and/or country where published.	
TD	C1	German Office Action dated October 24, 2006 [cited in claimed corresponding German Application No. DE 102 26 915.7].
TD	C2	Non-certified English translation of the German Office Action dated October 24, 2006.
TD	C3	Brück, Rainer, "Entwurfswerkzeuge für VLSI-Layout," "Methoden und Algorithmen für den rechnergestützten Entwurf von VLSI-Layout," pp. 140-143.
TD	C4	Non-certified English translation of the article by Brück, Rainer, "Entwurfswerkzeuge für VLSI-Layout," "Methoden und Algorithmen für den rechnergestützten Entwurf von VLSI-Layout," pp. 140-143.
TD	C5	Bourai et al., "Layout Compaction for Yield Optimization via Critical Area Minimization," Electrical Engineering Department, University of Washington, ACM, 2000, pp. 122-125.

EXAMINER <i>Mundo</i>	DATE CONSIDERED 11-06-2007
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.